IN THE SPECIFICATION:

Please amend the first full paragraph on page 2 as follows:

This application is a continuation of U.S. Patent Application Serial No. 09/146,742, filed on September 3, 1998, now U.S. Patent No. 6,348,411 issued February 19, 2002, whose amended title is "Method of Making a Contact ~~Structure",~~ Structure," of which a divisional Patent Application Serial Number 09/300,363 was filed on April 26, 1999, now U.S. Patent No. 6,740,916 issued May 25, 2004, with the title "Contact ~~Structure",~~ Structure," both of which are incorporated herein by reference.

Please amend the third full paragraph on page 2 as follows:

As microchip technology continues to increase in complexity and decrease in component size, dimensions are shrinking to the quarter micron scale and smaller. With use of the current high-yield photolithographic techniques, the margin of error has become increasingly tighter such that a single misaligned fabrication step can cause an entire chip to be flawed and be discarded. As devices shrink further, overstepping each process step's window of error increases the likelihood of fabrication failure. ~~A production worthy~~ production-worthy device feature requires incidental skill of a process engineer and a fabrication operator to fabricate the feature.

Please amend the paragraph bridging pages 2 and 3 as follows:

One device that is subject to the ever-increasing pressure to miniaturize is the dynamic random access memory (DRAM). DRAMs comprise arrays of memory cells ~~which~~ that contain two basic components--a field effect access transistor and a capacitor. Typically, one side of the transistor is connected to one side of the capacitor. The other side of the transistor and the transistor gate electrode are connected to external connection lines called a bit line and a word line, respectively. The other side of the capacitor is connected to a reference voltage. Therefore, the formation of the DRAM memory cell comprises the formation of a transistor, a capacitor and contacts to external circuits.

Please amend the first full paragraph on page 3 as follows:

It is advantageous to form integrated circuits with smaller individual elements so that as many elements as possible may be formed in a single chip. In this way, electronic equipment becomes smaller, assembly and packaging costs are minimized, and integrated circuit performance is improved. The capacitor is usually the largest element of the integrated circuit chip. Consequently, the development of smaller DRAMs focuses to a large extent on the capacitor. Three basic types of capacitors are used in DRAMs -- planar capacitors, trench capacitors, and stacked capacitors. Most large capacity DRAMs use stacked capacitors because of their greater capacitance, reliability, and ease of formation. For stacked capacitors, the side of the capacitor connected to the transistor is commonly referred to as the "storage ~~node",~~ node," and the side of the capacitor connected to the reference voltage is called the cell plate. The cell plate is a layer that covers the entire top array of all the ~~substrate-connected~~ substrate-connected devices, while there is an individual storage node for each respective storage bit site.

Please amend the paragraph bridging pages 3 and 4 as follows:

The areas in a DRAM to which an electrical connection is made are the gate of a transistor of the DRAM, a contact plug to an active area, and the active area itself. Active areas, which serve as source and drain regions for transistors, are discrete specially doped regions in the surface of the silicon substrate. A bit line contact corridor (BLCC) is created in order to make electrical connection to an active area. The BLCC is an opening created through the insulating material separating the bit line and the active area. The BLCCs are filled with a conductive material, such as doped polysilicon, doped Al, AlSiCu, or Ti/TiN/W. Before filling the BLCC, however, a process engineer must design a process flow for fabricating the BLCC that assures that the BLCC is not ~~misaligned, and therefore~~ misaligned and, therefore, not prone to shorting out or subject to errant charge leaking due to an exposed cell plate in the BLCC.

Please amend the second full paragraph on page 4 as follows:

As the size of the DRAM is reduced, the size of the active areas and the BLCCs available for contacts to reach the active areas are also reduced. Every process step has its own alignment limitations. While alignment is not exact between process steps, strict tolerances are required in order to accomplish a corridor that avoids a short between a contact that will be deposited in the BLCC and any other conductive materials ~~(i.e.~~ (i.e., cell plate to active area). Hence, it is desirable to effectively isolate the contacts from the transistor and capacitor components while optimizing the space available to make the contacts.

Please amend the third full paragraph on page 4 as follows:

The conventional methods of forming contacts between bit lines ~~and an~~ and active areas experience alignment problems in avoiding a short circuit between the electrically conductive bit line contact and the cell plate or storage node of a capacitor.

Please amend the first full paragraph on page 5 as follows:

A method and structure is disclosed that are advantageous for preventing shorting of a contact to an active area with a capacitor cell plate and a capacitor storage node. In accordance with one aspect of the invention, a method of fabricating a DRAM is disclosed that utilizes an insulated sleeve structure to self-align a bit line contact corridor (BLCC) to an active area of a DRAM transistor. In accordance with this aspect of the invention, capacitors are formed over a semiconductor substrate. In the context of this document, the term "semiconductor substrate" is defined to mean any construction comprising semiconductive ~~material, including~~ material including, but not limited ~~to~~ to, bulk semiconductive material such as a semiconductive wafer, either alone or in assemblies comprising other materials thereon, and semiconductive material layers, either alone or in assemblies comprising other materials. The term "substrate" refers to any supporting structure ~~including~~ including, but not limited ~~to~~ to, the semiconductor substrates described above.

Please amend the second full paragraph on page 5 as follows:

In the inventive method, a lower bulk insulator layer is formed upon the semiconductor ~~substrate,~~ substrate and a dielectric layer is formed upon the lower bulk insulator layer. Next, a conductor layer is formed upon the dielectric layer and an upper bulk insulator layer is formed upon the conductor layer. An etch is performed to selectively remove the conductor layer, the dielectric layer, and the lower bulk insulator layer so as to form an opening defined by the lower bulk insulator layer, the dielectric layer, and the conductor layer. The opening terminates at a bottom surface within the lower bulk insulator layer above the semiconductor substrate.

Please amend the paragraph bridging pages 5 and 6 as follows:

Next, a sleeve insulator layer is deposited upon the upper bulk insulator layer and within the opening so as to make contact with each of the lower bulk insulator layer, the dielectric layer, and the conductor layer. An etch process is then performed to substantially remove the sleeve insulator layer from the bottom surface within the lower bulk insulator layer above the semiconductor ~~substrate,~~ substrate and from on top of the insulator layer, thus leaving the sleeve insulator layer in contact with each of the lower bulk insulator layer, the dielectric layer, and the conductor layer.

Please amend the second full paragraph on page 6 as follows:

The sleeve insulator layer, which ~~self-aligns~~ self-aligns the BLCC, allows for improved alignment tolerances between the BLCC and other layers, thus preventing errant charge leakage and short circuits between the conductive plug formed within the BLCC and the other layers.

Please amend the third full paragraph on page 6 as follows:

Conceptually, the etching of the BLCC progressively deeper into the lower bulk insulator layer can be carried out incrementally with a plurality of depositions of the material of the sleeve insulator layer, ~~each said~~ each deposition being followed by an etch of the sleeve insulator layer to remove the same from the bottom of the BLCC within the lower bulk insulator layer.

Please amend the first full paragraph on page 7 as follows:

A more particular description of the invention briefly described above will be rendered by reference to specific embodiments ~~thereof~~ thereof, which are illustrated in the appended drawings. Understanding that these drawings depict only typical embodiments of the invention and are ~~not therefore~~ not, therefore, considered to be limiting of its scope, the invention will be described and explained with additional specificity and detail through the use of the accompanying drawings in which:

Please amend the second full paragraph on page 7 as follows:

Figures 1-5 are ~~cross-section~~ cross-sectional views of a DRAM memory cell undergoing fabrication according to a first embodiment of the present invention.

Please amend the first full paragraph on page 9 as follows:

An embodiment of the invention will now be described with reference to Figures ~~1-9.~~ 1-9. Referring to Figure 1, a semiconductor substrate 10 comprises a silicon substrate 12 with a gate insulating layer 14, field oxide regions 16, active or source/drain regions 18a and 18b, and access transistors 20. Each access transistor 20 has a gate electrode 24, one or more insulating protective ~~layer 28,~~ layers 26 and 28, and insulating spacers 30 that are formed on the sides thereof. A lower bulk insulator layer 36 is then deposited and if necessary, planarized. Lower bulk insulator layer 36 is preferably made of a dielectric material such as borophosphosilicate glass (BPSG), phosphosilicate glass (PSG), borosilicate glass (BSG), or spin on glass (SOG).

Please amend the fourth full paragraph on page 9 as follows:

Referring to Figure 5, a capacitor cell dielectric layer 44 is deposited. Capacitor cell dielectric layer 44, which is intended to form a portion of dielectric material for a capacitor, is preferably made of Si_3N_4 or other electrically insulative suitable material such as Ta_2O_5, or

barium strontium titanate (BST). A cell plate layer 46 is then deposited. Cell plate layer 46 is intended to form a cell plate portion of a capacitor in an integrated circuit.

Please amend the paragraph bridging pages 10 and 11 as follows:

Referring to Figure 8, the next step of the present invention method is carried out in which the remaining portions of photoresist layer 60 have been removed, and then a sleeve insulator layer 50 is deposited upon the uppermost surface of cell plate insulating layer 48 and also within the BLCC. An ambient pressure chemical vapor deposition (CVD) process can be used to assist in lateral deposition of sleeve insulator layer 50 upon the sidewalls of the BLCC. Other methods, however, can be employed ~~which~~ that are calculated to achieve suitably conformal depositions. A preferred CVD substance for sleeve insulator layer 50 is Si_3N_4, SiO_2 (by decomposition of a tetraethylorthosilicate precursor), Ta_2O_5, or barium strontium titanate (BST), although the etchant used to etch lower bulk insulator layer 36 should be selective to the substance of sleeve insulator layer 50.

Please amend the first full paragraph on page 11 as follows:

Referring to Figure 9, a second etch step, which is anisotropic, is carried out to remove substantially all of the ~~horizontally exposed~~ horizontally exposed portions of sleeve insulator layer 50 from the bottom of the partially formed BLCC. Sleeve insulator layer 50 thus covers the exposed portions of capacitor cell dielectric layer 44, cell plate layer 46, and cell plate insulating layer 48 that are within contact hole 70.

Please amend the second full paragraph on page 11 as follows:

The structure represented in Figure 9 illustrates a first embodiment of the present invention wherein sleeve insulator layer 50 is formed into a hardened vertical sleeve and cell plate insulating layer 48 is formed into a horizontal plate. As such, sleeve insulator ~~layer 50,~~ layer 50 with cell plate insulating layer 48 function as a self-aligning contact site that will resist being removed in a subsequent etch step that etches the remainder of lower bulk insulator

layer 36. Such an etch of lower bulk insulator layer 36 will form a conduit from the upper surface of cell plate insulating layer 48 to the upper surface of the semiconductor substrate, and will not expose cell plate layer 46 at the edges of the BLCC. Sleeve insulator layer 50 will thereby insulate cell plate layer 46 from the effects of errant charge leakage and from shorting once the BLCC is filled with conductive material and put into service as a bit line contact. The embodiment of the invention seen in Figure 9 is not limited to bit line contact formation, but can be used where ~~self-aligned~~ self-aligned contacts are desirable, such as contacts to an active region, a transistor gate, or to a contact plug.

Please amend the paragraph bridging pages 11 and 12 as follows:

Figure 10 illustrates an example of a second embodiment of the present invention. Cell plate layer 46 maximizes its capacitative effect upon storage node layer 42 by its being wrapped conformally around two opposing vertical faces of storage node layer 42. In this embodiment, the cell-to-cell bridging of cell plate layer 46 is deeper in the structure. A ~~primary insulator~~ cell plate insulating layer 48 is deposited upon an upper bulk insulator layer 51. Then, a partial etch is made through ~~primary insulator~~ cell plate insulating layer 48 into upper bulk insulator layer 51 and stopping within a lower bulk insulator layer 36 so as to form a contact hole 70. A secondary sleeve insulator layer 50 is then deposited upon ~~primary insulator~~ cell plate insulating layer 48 and within contact hole 70. An anisotropic etch removes secondary sleeve insulator layer 50 from the bottom of contact hole 70 and other laterally exposed portions thereof. The anisotropic etch stops on insulator layer 48, leaving secondary sleeve insulator layer 50 as a liner on the sidewalls of contact hole 70. A subsequent opening can be formed to provide a contact to active region 18B and a contact plug is formed through secondary sleeve insulator layer 50 and in contact with active region 18b.

Please amend the second full paragraph on page 13 as follows:

Figures 12-14 illustrate the function of the first embodiment of the present invention as it provides a self-aligning contact hole site for further processing. Referring to Figures 12-14, there

are illustrated qualitative process flow examples of both proper alignment and misalignment in the formation of a contact plug in a contact hole. The misalignment example is set forth to illustrate the ~~self-alignment~~ self-alignment feature of the invention.

Please amend the third full paragraph on page 13 as follows:

Figure 12 shows large and small off-set alignment circles 82, 86 ~~which~~ that are meant to indicate an etching process through a layer of insulation material (not shown) above cell plate insulating layer 48 so as to form contact hole 70 defined within sleeve insulator layer 50. A center line 83 represents the axis through the center of small off-set alignment circle 82, and a center line 87 represents the axis through the center of large off-set alignment circle 86. As seen in Figure 12, center line 83 and center line 87 are off set one from the other. A center line 71 represents the axis ~~defining the~~ of contact hole 70.

Please amend the fourth full paragraph on page 13 as follows:

Small off-set alignment circle 82 shows a misalignment distance Δ_1 from center line 83 to center line 71. Large off-set alignment circle 86 shows a misalignment distance Δ_2 from center line 87 to center line 71. The ~~self-alignment~~ self-alignment of the etch process to form contact hole 70 is due to the selectivity of the etchant in the etch process to both sleeve insulator layer 50 and cell plate insulating layer 48 as the etch process etches lower bulk insulator ~~layer 36~~ layer 36, which defined the termination of contact hole 70.

Please amend the paragraph bridging pages 13 and 14 as follows:

Figure 13 shows that an upper bulk insulator layer 51 is deposited within the area defined by sleeve insulator layer 50 and upon cell plate insulating layer 48. A patterned photoresist ~~layer 56~~ layer 60 has been formed upon upper bulk insulator layer 51. The pattern in patterned photoresist ~~layer 56~~ layer 60 is intended to be aligned with respect to sleeve insulator layer 50 so that a subsequent etch will open a contact through upper bulk insulator layer 51 and lower bulk insulator layer 36 to expose a contact on active area 18b. Patterned photoresist ~~layer 56,~~

layer 60, however, may be misaligned with respect to sleeve insulator layer 50, as was illustrated by the foregoing discussion of Figure 12.

Please amend the first full paragraph on page 14 as follows:

The etch through patterned photoresist ~~layer 56~~ layer 60 forms the BLCC via contact hole 70 seen in Figures 14-15. It is desirable that contact hole 70, which extends to active area 18b through sleeve insulator layer 50, is formed such that the BLCC is in alignment with contact hole 70 through cell plate layer 46. When so aligned, the etch has a diameter d seen in Figure 12 which extends to the sidewall of sleeve insulator layer 50, and the largest possible contact to active area 18b is achieved. Sleeve insulator layer 50 enables the inventive method to form sub-photolithography resolution limit critical dimensions, such as is seen in Figure 12.

Please amend the paragraph bridging pages 14 and 15 as follows:

Figure 14 demonstrates that, although the etch hole is misaligned with respect to sleeve insulator layer 50, the etch is still ~~self aligned~~ self-aligned with sleeve insulator layer 50 due to the selectivity of the etch with respect to the material from which sleeve insulator layer 50 is composed and due to the etch selectivity to the material of which cell plate insulating layer 48 is composed. The self-alignment of the etch through sleeve insulator layer 50 and the stopping of the etch on cell plate insulating layer 48 in effect assures an electrical insulation of cell plate layer 46 that prevents an electrical short with an electrically conductive bit line contact 92 within the BLCC. Bit line contact 92, which is preferably a conductive plug, can be formed by filling the BLCC with tungsten ~~deposited,~~ deposited by chemical vapor ~~deposition,~~ deposition with germanium-doped aluminum reflowing, and with other materials and processes. Additionally, a refractory metal silicide may be formed at the bottom of the BLCC upon active area 18b. After the material forming bit line contact 92 has been formed within contact hole 70, a planarizing operation may be conducted to confine the material of bit line contact 92 within contact hole 70 as illustrated in Figures 14-15.

Please amend the second full paragraph on page 15 as follows:

The process creating the structure seen in Figure 14 is substantially the same as that creating the structure seen in Figure 15. In Figure 15, a circle 90 illustrates in phantom a cross-section of an etch hole through upper bulk insulator layer 51. The etch hole is aligned with respect to sleeve insulator layer 50. Also, the etch is ~~self-aligned~~ self-aligned with sleeve insulator layer 50 due to the selectivity of the etch with respect to the material from which sleeve insulator layer 50 is substantially composed, and due to the etch selectivity to the material of which cell plate insulating layer 48 is composed. As was described with respect to Figure 13, the self-alignment of the etch through sleeve insulator layer 50 in effect assures electrical insulation of cell plate layer 46 to prevent an electrical short with electrically conductive bit line contact 92 within the BLCC. Figure 15 illustrates the maximum contact size on active area 18b, as dictated by the diameter of the area defined within sleeve insulator layer 50. Electrical insulation protection of bit line contact 92 is provided by cell plate insulating layer 48 and sleeve insulator layer 50 so as to prevent shorting of cell plate layer 46 with bit line contact 92.

Please amend the first full paragraph on page 16 as follows:

Figure 16 shows the divergent types of contacts that can be made using the invention, although all of the depicted contacts need not be present in the same structure nor be situated as depicted in Figure 16. In Figure 16, circle 90 illustrates in phantom a ~~cross-section~~ cross-section of an etch hole, made by conventional etch processes, through upper bulk insulator layer 51. A contact plug 72 is upon source/drain region 18b. Electrically conductive bit line contact 92 is situated within contact hole 70 and passes through sleeve insulator ~~layer 50~~ layer 52 to terminate upon contact plug 72. Circle 94 illustrates in phantom a cross-section of a contact hole 98, made by conventional etch processes, through upper bulk insulator layer 51 and into a transistor so as to stop on a gate electrode 24 beneath an insulating protective layer 28 of a transistor. Electrically conductive contact 100 is situated within contact hole 98 and passes through a sleeve insulator layer 52 to make contact with gate electrode 24. Circle 104 illustrates in phantom a cross-section of a contact hole 106,

made by conventional etch processes, through upper bulk insulator layer 51 and into storage node layer 42. Electrically conductive contact 102 is situated within contact hole 106 and passes through a sleeve insulator layer 53 to make contact with storage node layer 42. Sleeve insulator layer 53 insulates electrically conductive contact 102 from cell plate layer 46.

Please amend the paragraph bridging pages 16 and 17 as follows:

~~A~~ The fifth and sixth ~~embodiment~~ embodiments of the present invention, illustrated respectively in Figures 10 and 11, ~~comprises~~ comprise a larger surface area deposition of cell plate layer 46 that requires a deeper penetrating partial etch to create the self-aligning feature. These embodiments vary from the fourth embodiment in that a selective etch step is required to remove most of lower bulk insulator layer 36 so as to expose external lateral surfaces of cell plate layer 46. In the fifth ~~embodiment,~~ embodiment seen in Figure 10, upper bulk insulator layer 51 is deposited and planarized and then a sleeve insulator layer 50 is deposited upon upper bulk insulator layer 51 and within contact hole 70. As was discussed above, a conductive plug (not shown) is formed within contact hole 70 once an etch exposes active area 18b. The conductive plug is electrically insulated from cell plate layer 46 by sleeve insulator layer 50 and could also be so insulated by primary insulator layer 48. The sixth embodiment, seen in ~~Figure 11,~~ Figure 11 differs from the fifth ~~embodiment,~~ embodiment seen in ~~Figure 10,~~ Figure 10 in that a cell plate insulating layer 48 is over cell plate layer 46 for off-site coverage where it is useful or ~~not convenient~~ inconvenient to mask out deposition upon cell plate layer 46.

Please amend the first full paragraph on page 17 as follows:

Other materials, structures, and processes may be substituted for the particular ones described. For example, silicon nitride, preferably Si_3N_4, may be used instead of silicon dioxide for insulating protective layer 28 and spacers 30. Spin-On Glass (SOG), polyamide insulator (PI), chemical ~~vapor deposited~~ vapor-deposited (CVD) oxide or other insulators such as boron silicate glass (BSG) or phosphosilicate glass (PSG) may be used in place of ~~boro phospho silicate~~ borophosphosilicate glass (BPSG) for lower bulk insulator layer 36.

Other satisfactory materials may be substituted for any of the ~~above. Or,~~ above or additional materials, structures, and processes may also be added to those disclosed.

Please amend the second full paragraph on page 17 as follows:

The present invention may be embodied in other specific forms without departing from its spirit or essential characteristics. The described embodiments are to be considered in all respects only as illustrated and not restrictive. The scope of the invention is, therefore, indicated by the appended claims and their whole or partial combination rather than by the foregoing description. All changes ~~which~~ that come within the meaning and range of equivalency of the claims are to be embraced within their scope.